AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 1 and 9 without prejudice. Please add new claims 22 and 23.

1. (CANCELED)

2. (CURRENTLY AMENDED) The circuit according to claim 5~~1~~, wherein said first controller is further configured to set said first semaphore to said free status in response to said processor writing to said first address.

3. (CURRENTLY AMENDED) The circuit according to claim 5~~1~~, wherein said first controller is further configured to present said status of said first semaphore in response to said processor reading a second address.

4. (CURRENTLY AMENDED) The circuit according to claim 3, wherein said first controller is further configured to maintain said status of said semaphore in response to said processor writing to said second address.

5. (PREVIOUSLY PRESENTED) A circuit comprising:

a first memory element defining a first semaphore allocatable to a resource; and

a first controller configured to (i) present a granted status in response to a processor reading a first address while said first semaphore has a free status, (ii) set said first semaphore to a busy status in response to presenting said granted status and (iii) present said busy status in response to said processor reading said first address while said first semaphore has said busy status; and

a second memory element defining a second semaphore allocatable to said first semaphore.

6. (PREVIOUSLY PRESENTED) The circuit according to claim 5, wherein said first controller is further configured to (i) slave said first semaphore to said second semaphore, (ii) present said busy status in response to said processor reading said first address while said second semaphore has said busy status and (iii) maintain said busy status for said first semaphore in response to said processor writing to said first address while said second semaphore has said busy status.

7. (PREVIOUSLY PRESENTED) The circuit according to claim 6, wherein said first controller is further configured to set said first semaphore to said free status in response to said processor writing to a second address.

8. (PREVIOUSLY PRESENTED) The circuit according to claim 6, wherein said first controller is further configured to

maintain said busy status for said first semaphore in response to said processor writing to a second address.

9. (CANCELED)

10. (CURRENTLY AMENDED) The method according to claim 13~~9~~, further comprising the step of setting said first semaphore to said free status in response to said processor writing to said first address.

11. (CURRENTLY AMENDED) The method according to claim 13~~9~~, further comprising the step of presenting said status of said first semaphore in response to said processor reading a second address.

12. (CURRENTLY AMENDED) The method according to claim 11, further comprising the step of maintaining said status of said first semaphore in response to said processor writing to said second address.

13. (PREVIOUSLY PRESENTED) A method of allocating a resource to a processor, comprising the steps of:

(A) defining a first semaphore allocatable to said resource;

(B) presenting a granted status in response to said processor reading a first address while said first semaphore has a free status;

(C) setting said first semaphore to a busy status in response to presenting said granted status;

(D) presenting said busy status in response to said processor reading said first address while said first semaphore has said busy status; and

(E) defining a second semaphore allocatable to said first semaphore.

14. (CURRENTLY AMENDED) The method according to claim 13, further comprising the ~~steps~~ step of:

slaving said first semaphore to said second semaphore~~;~~

~~presenting said busy status in response to said processosr reading said first address while said second semaphore has said busy status; and~~

~~maintaining said busy status for said first semaphore in response to said processor writing to said first address while said second semaphore has said busy status~~.

15. (CURRENTLY AMENDED) The method according to claim 23~~14~~, further comprising the step of:

setting said first semaphore to said free status in response to said processor writing to a second address.

16. (CURRENTLY AMENDED) The method according to claim 23~~14~~, further comprising the step of:

maintaining said busy status for said first semaphore in response to said processor writing to a second address.

17. (CURRENTLY AMENDED) A circuit comprising:

means for defining a first semaphore allocatable to a resource;

means for presenting a granted status in response to a processor reading a first address while said first semaphore has a free status;

means for setting said first semaphore to a busy status in response to presenting said granted status; ~~and~~

means for presenting said busy status in response to said processor reading said first address while said first semaphore has said busy status; and

means for defining a second semaphore allocatable to said first semaphore.

18. (PREVIOUSLY PRESENTED) The circuit according to claim 5, further comprising a second controller configured to (i) present said granted status in response to said processor reading a second address while said second semaphore has said free status, (ii) set said second semaphore to said busy status in response to presenting said granted status and (iii) present said busy status

in response to said processor reading said second address while said second semaphore has said busy status.

19. (PREVIOUSLY PRESENTED) The circuit according to claim 18, wherein said second controller is further configured to set said second semaphore to said free status in response to said processor writing to said second address.

20. (PREVIOUSLY PRESENTED) The method according to claim 13, further comprising the steps of:

second presenting said granted status in response to said processor reading a second address while said second semaphore has said free status;

setting said second semaphore to said busy status in response to said second presenting of said granted status; and

presenting said busy status in response to said processor reading said second address while said second semaphore has said busy status.

21. (PREVIOUSLY PRESENTED) The method according to claim 20, further comprising the step of:

setting said second semaphore to said free status in response to writing to said second address.

22. (NEW) The method according to claim 14, further comprising the step of:

presenting said busy status in response to said processosr reading said first address while said second semaphore has said busy status.

23. (NEW) The method according to claim 22, further comprising the step of:

maintaining said busy status for said first semaphore in response to said processor writing to said first address while said second semaphore has said busy status.